

Tears for fears

Breaking an RFID counter

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Outline:

1. Introduction
2. Counter
3. Exploit
4. Results

AMOSSYS

Information Technology Security Evaluation Facility
(ITSEF)
Software evaluation

Introduction

01.

Our goal was to reproduce state-of-the-art attack presented by Quarkslab in 2021 at SSTIC.

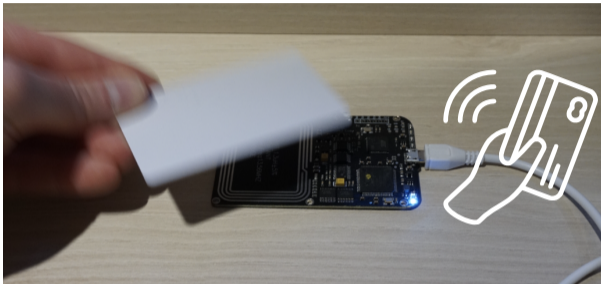
Quarkslab

- Targets NXP Cards
- Provides a methodology
- Provides tools

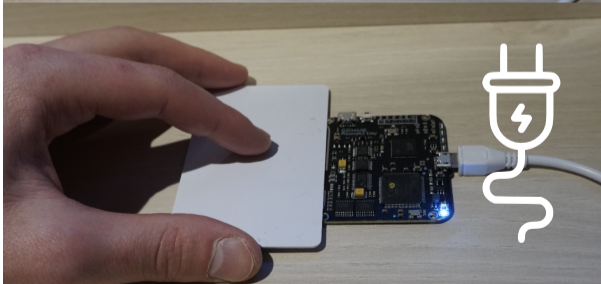
Our contribution

- Targets ST25TB* Cards
- Adapts their methodology

¹C. Herrmann P. Teuwen. *EEPROM: It Will All End in Tears*.



Physical Removal
Cards designed to resist

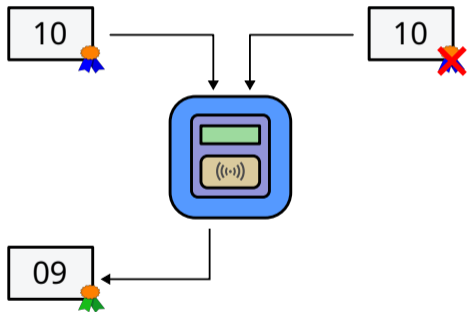


Reader shutdown
What could go wrong ?

A Proxmark and Iceman's
firmware is recommended

Address	ST25TB04K	ST25TB02K	ST25TB512-AC	ST25TB512-AT
[0:4]	Resettable OTP			Lockable EEPROM
[5:6]	Monotonic Counters			
[7:15]	Lockable EEPROM			
[16:23]	EEPROM	EEPROM		
[64:127]				
255	System OTP bits			
UID0	64 bits UID ROM D0 02 1F + serial	64 bits UID ROM D0 02 3F + serial	64 bits UID ROM D0 02 1B + serial	64 bits UID ROM D0 02 33 + serial
UID1				

Exploit tested on ST25TB512-AT, rest of the family confirmed vulnerable by ST.



Notes:

Cards are signed

Each machine can sign

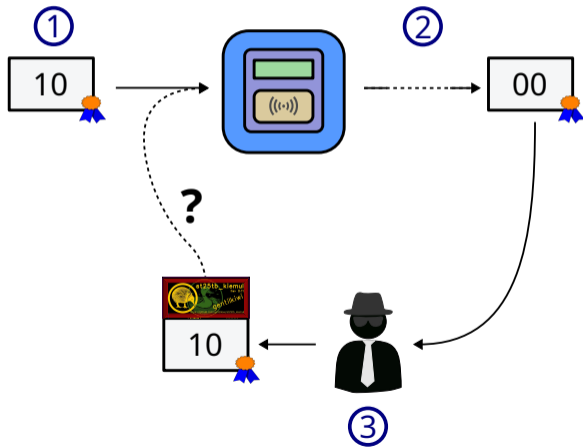
Cards must be valid

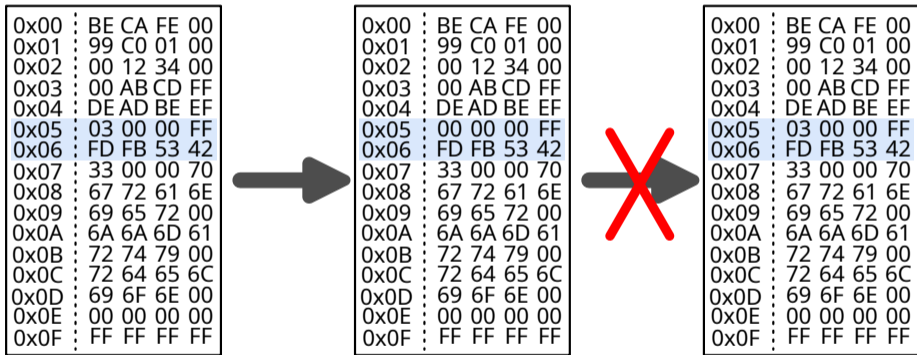
²Benjamin Delpy. *ST25TB series NFC tags for fun in French* public transports*, 2023.

Benjamin Delpy:

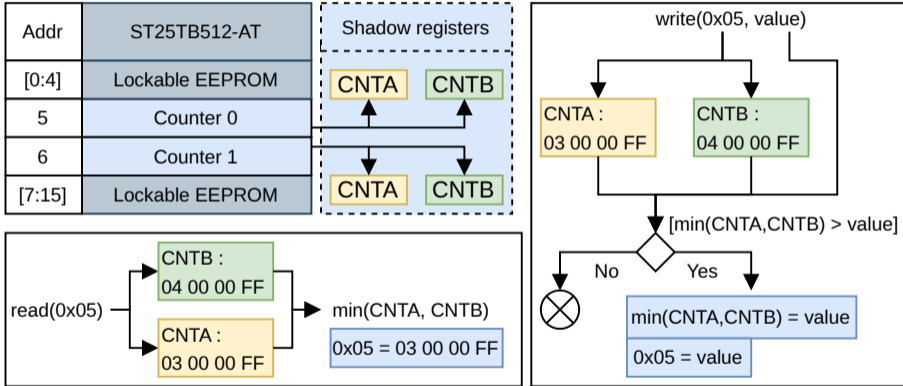
1. Read the card
2. Use the card
3. Restore the original state

⇒ Using an emulator





Impossible to reuse tickets because of the monotonic counters.



Logic based on observed counter behavior and patent : FR3103925B1

Counter relies on EEPROM memories, EEPROM write are not atomic.

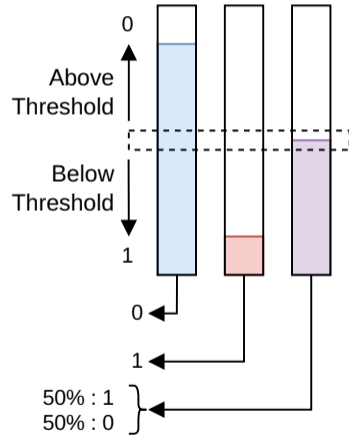
Write are block-wide (32 bits) and a two-step operation:

1. Erase everything (erased bits are logic 1)
2. Program bits (programed bits are logic 0)

EEPROM cells are analogic.

A cell has a logic value of:

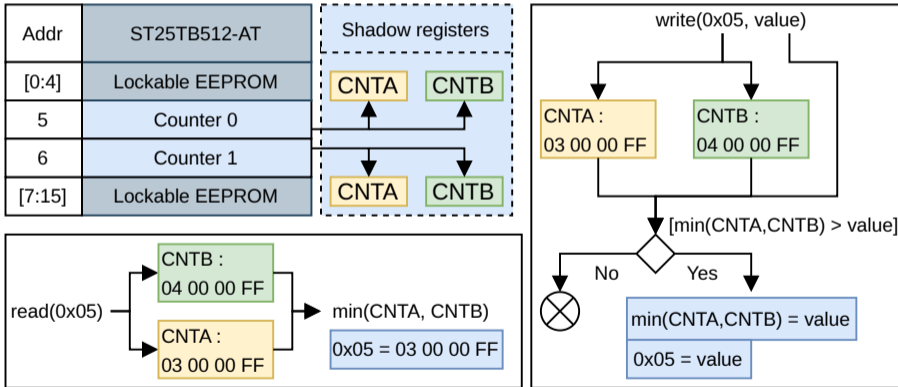
- [0] → Close to be full/programed
- [1] → Close to be emptied/erased
- [?] → **Weak bit**, probabilistic interpretation



Counter

02.

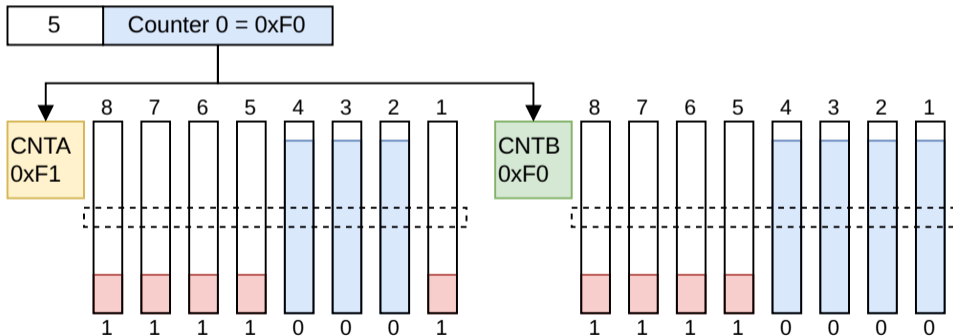
Counters use the following logic:



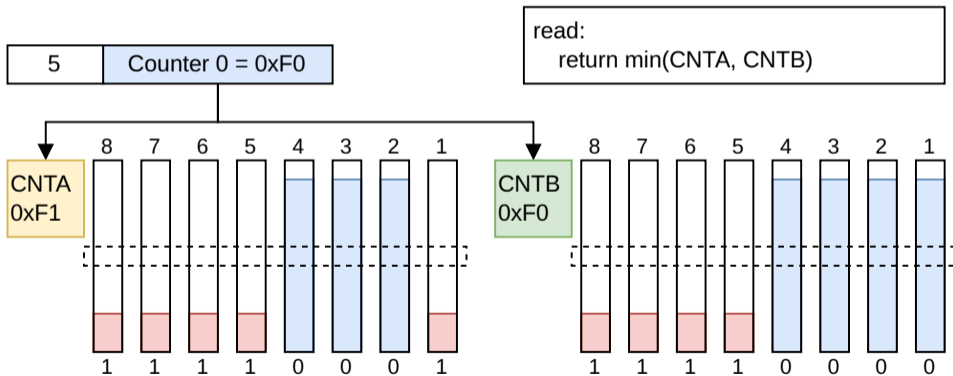
Based on observed counter behavior and patent : FR3103925B1

Counter architecture:

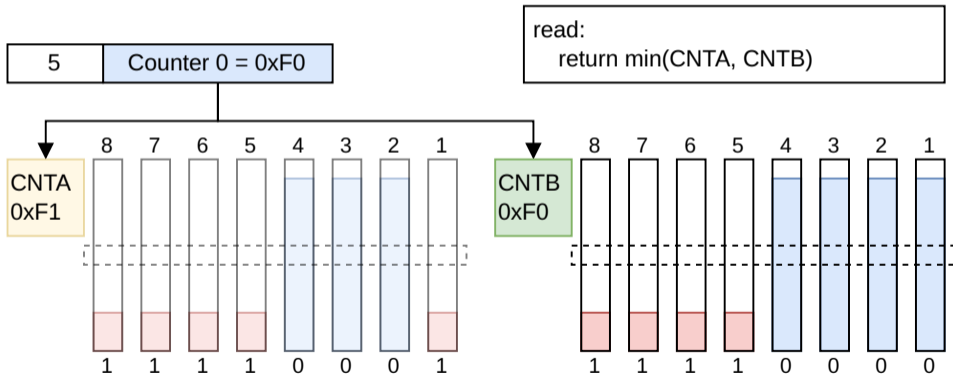
View truncated to first 8 bits, a bloc is 32 bits wide on ST25TB*.



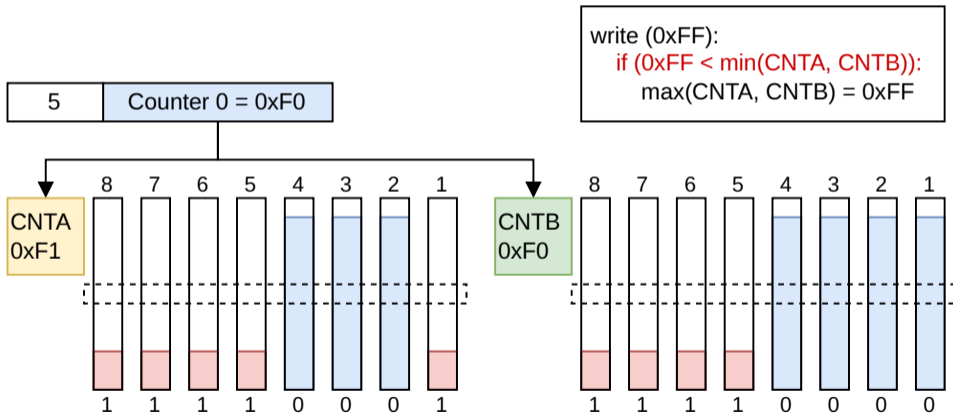
Example of a read on counter 5:



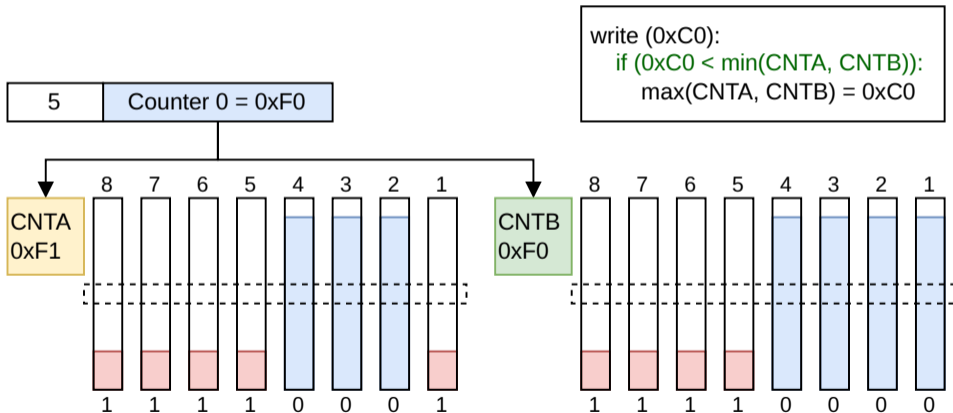
Example of a read on counter 5:



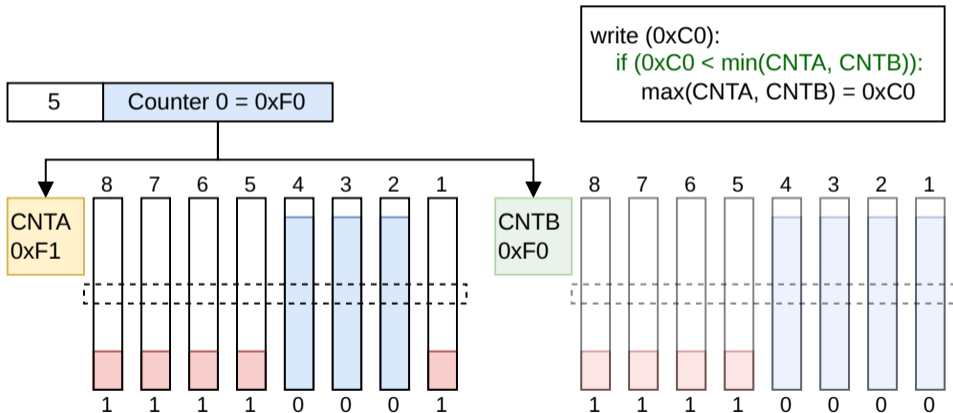
Example of a write(0xFF) on counter 5:



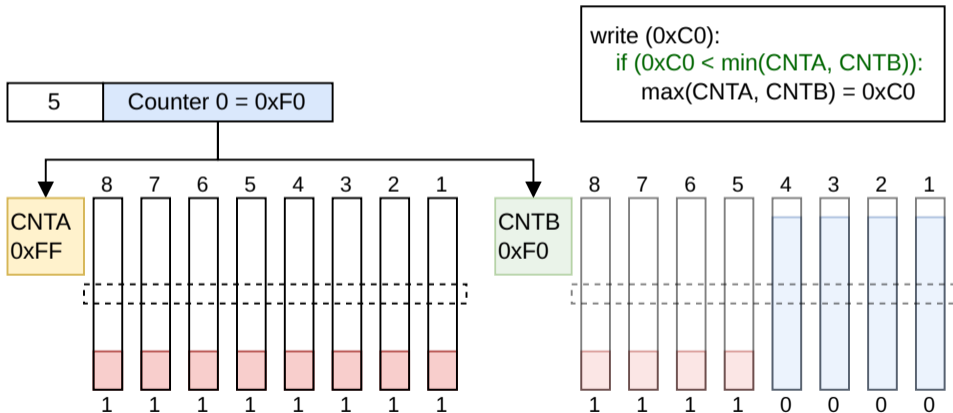
Example of a write(0xC0) on counter 5:



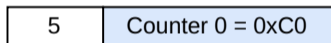
Example of a write(0xC0) on counter 5:



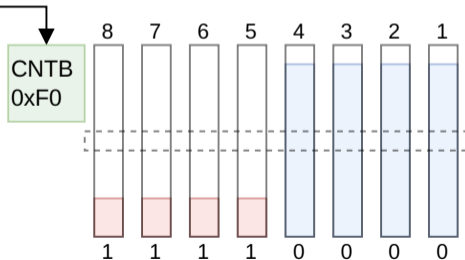
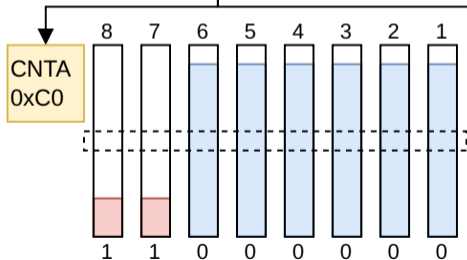
Example of a write(0xC0) on counter 5:



Example of a write(0xC0) on counter 5:



write (0xC0):
if (0xC0 < min(CNTA, CNTB)):
max(CNTA, CNTB) = 0xC0



At no point in a single interrupted write the counter value is compromised.

We need a trick to write 0xFF in **both** shadow registers.

Exploit's details

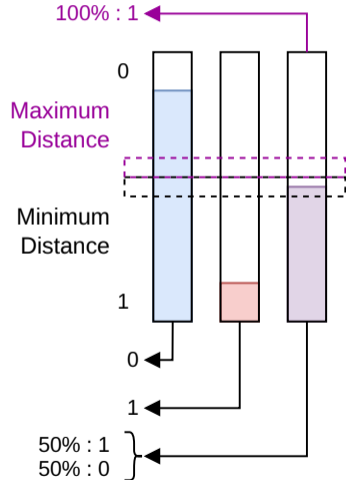
03. ■

Weak bit:

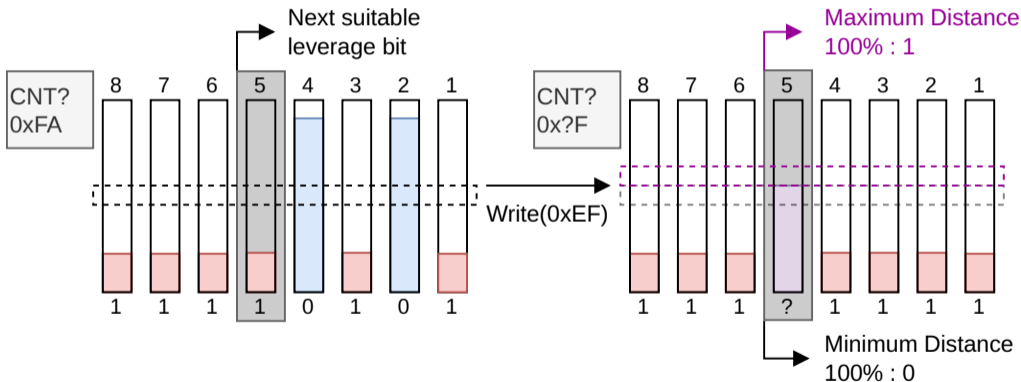
EEPROM cells close to the evaluation threshold have probabilistic interpretations.

Distance dependency:

When a card is far from its reader, weak bits are more likely to be interpreted at 1.



Set next power of 2 at 0, and the rest to 1, shape a weak bit.

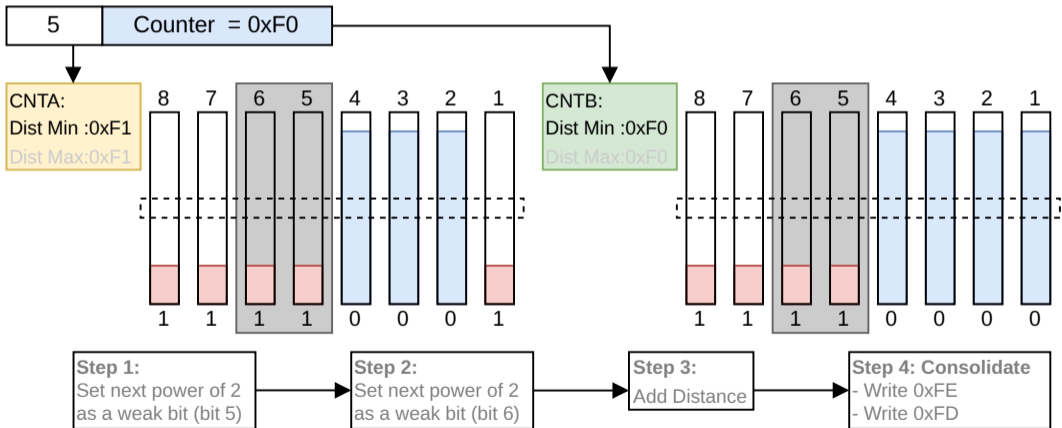


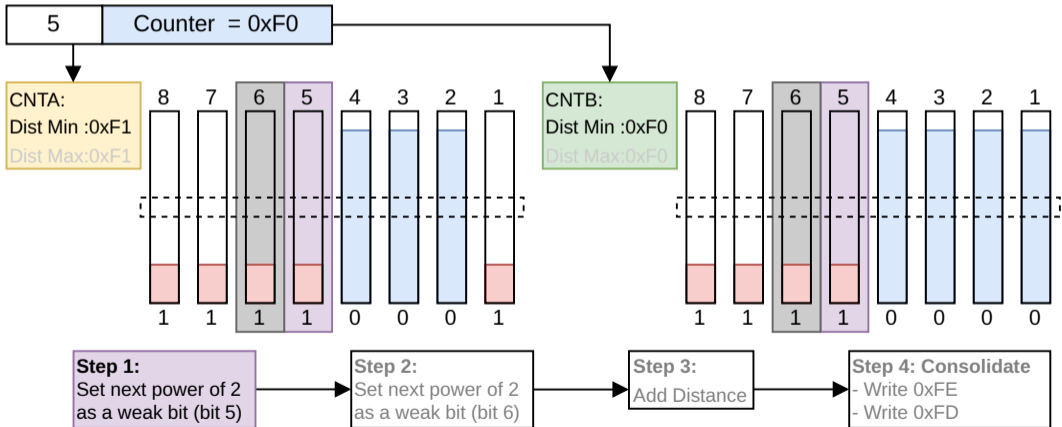
This kind of pattern is what we need to reset our counter.

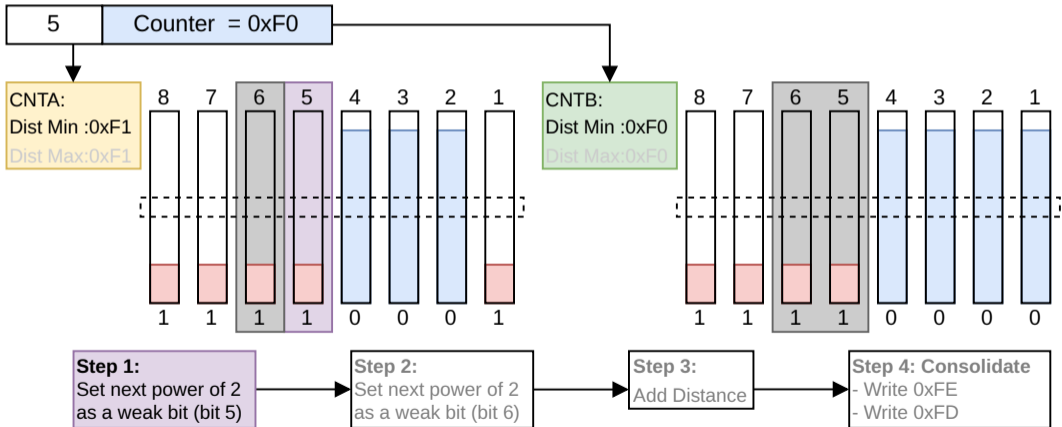


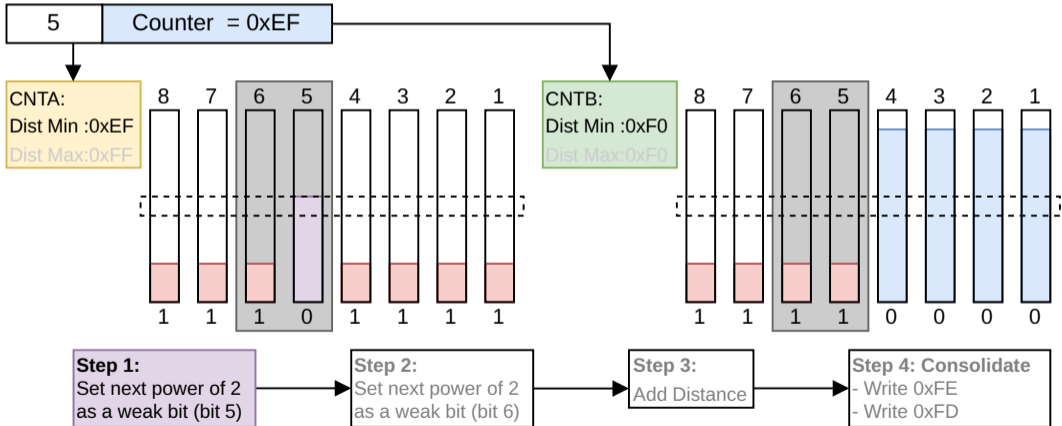
We use the previous gadget to control both sub-counter (Steps 1-2).

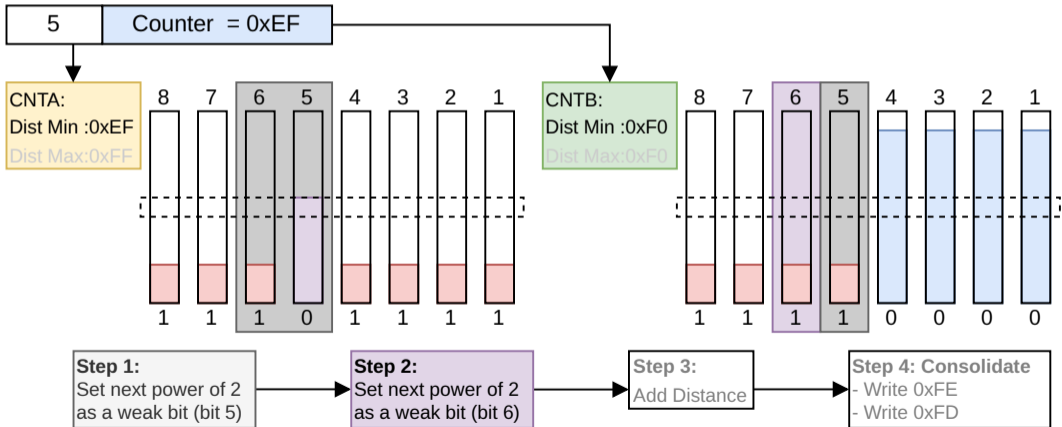
After adding distance we can write any arbitrary value and remove any weak bit (Steps 3-4).

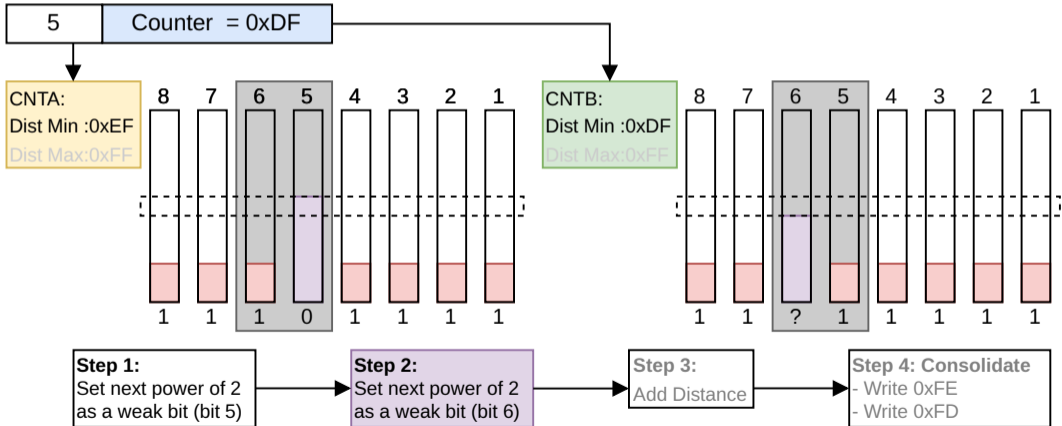


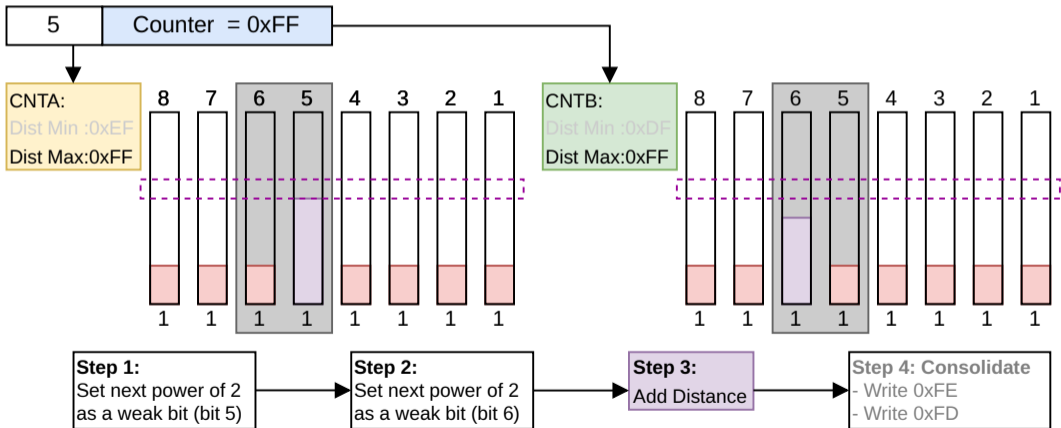


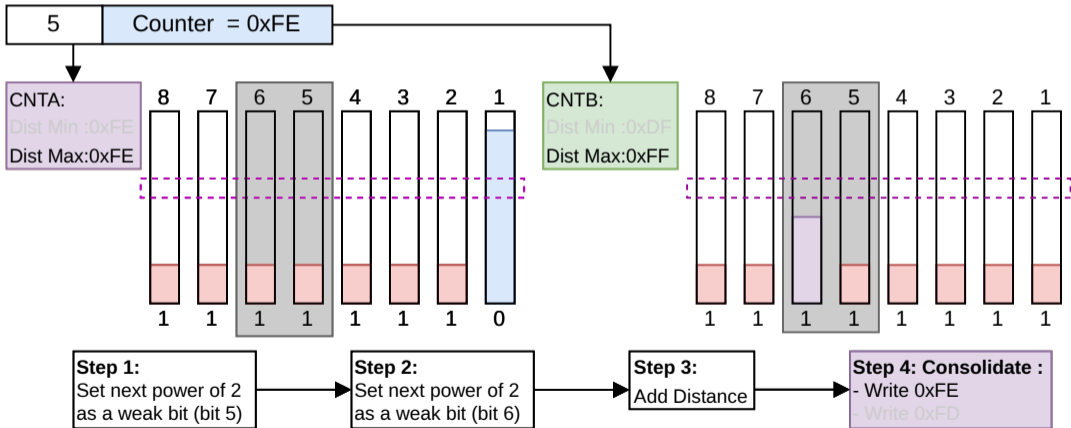


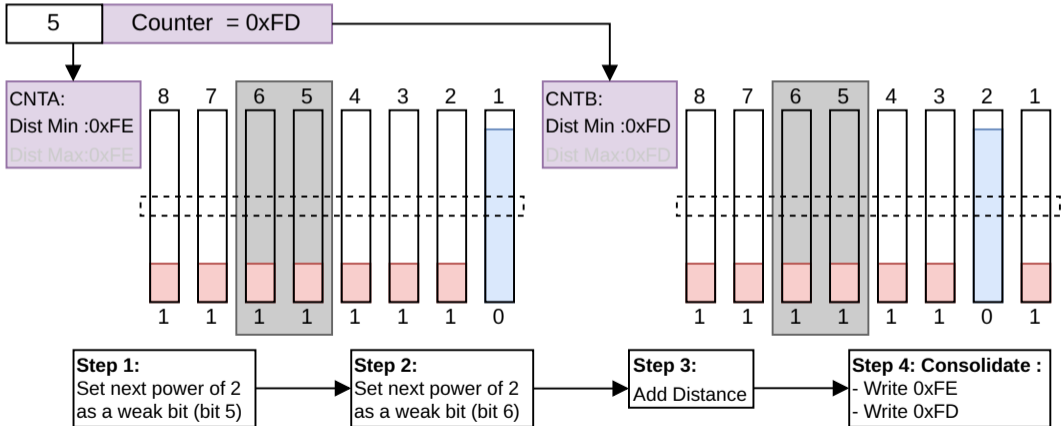












Results

04.

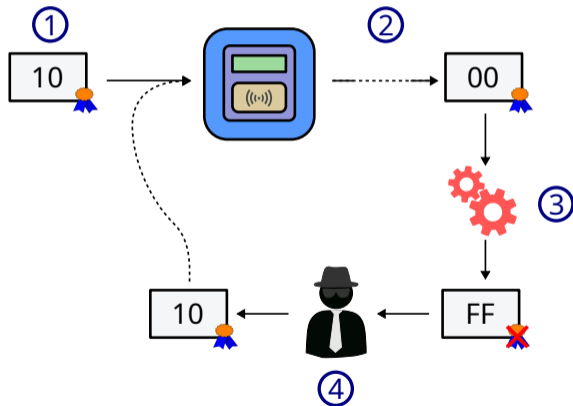
Some pitfalls and odd things.

- Timings a lot shorter for counter EEPROM vs standard blocs.
- How quickly operations are done influence weak bits interpretations.

Exploit sources at : <https://gitlab.com/SiliconOtter/tears4fears>

New version:

1. Read the card
2. Use the card
3. Increment the counters
4. Restore the original state





Don't forget:

Testing on production **is illegal**

Might be detected

Be responsible

Thanks for listening

